Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **OUT A**
2. **N/C**
3. **IN A**
4. **V –**
5. **IN B**
6. **N/C**
7. **OUT B**
8. **V +**

**.078”**

**.075”**

**8 8**

**3 5**

**1**

**4**

**7**

**4**

**MASK**

**REF**

**ICL7667M**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004” min.**

**Backside Potential:**

**Mask Ref: ICL7667M**

**APPROVED BY: DK DIE SIZE .075” X .078” DATE: 9/8/21**

**MFG: INTERSIL / HARRIS THICKNESS .019” P/N: ICL7667**

**DG 10.1.2**

#### Rev B, 7/1